**Listing of Claims:**

This listing of claims replaces all prior versions and listings of claims in the application:

1-17.(Canceled)

18.(Currently Amended) A method of making a flash memory cell comprising a floating gate with corners each having a sharp, upwardly flared shape, the method comprising the steps of:

providing a substrate of semiconductor material;

forming a mask film over the substrate;

defining a trench in the mask film, the trench terminating above the substrate;

at least partially filling the trench with a first film of electroconductive material; ~~and~~

etching back a portion of the first film of electroconductive material to form the floating gate with the sharp, upwardly flared corners;

at least partially filling the trench with a second film of the electroconductive material; and

etching back at least a portion of the second film of the electroconductive material to further sharpen and upwardly flare the corners of the floating gate.

19.(Canceled)

20.(Currently Amended) The method according to claim ~~19~~ 18, wherein the etching back step performed after the step of at least filling the trench with the second film of the electroconductive material etches back another portion of the first film of the electroconductive material.

21.(Original) The method according to claim 20, further comprising the step of at least partially filling the trench with a dielectric material to form a protective cap over the floating gate.

22.(Currently Amended) The method according to claim ~~19~~ 18, further comprising the step of at least partially filling the trench with a dielectric material to form a protective cap over the floating gate.

23.(Original) The method according to claim 18, further comprising the step of at least partially filling the trench with a dielectric material to form a protective cap over the floating gate.

24.(Original) The method according to claim 18, wherein the substrate includes at least two shallow trench electrical isolation regions and further comprising the step of removing selected additional portions of the first film of the electroconductive material covering the shallow trench electrical isolation regions to electrically isolate the cell.

25.(Currently Amended) The method according to claim ~~19~~ 18, wherein the substrate includes at least two shallow trench electrical isolation regions and further comprising the step of removing selected additional portions of the first film of the electroconductive material covering the shallow trench electrical isolation regions to electrically isolate the cell.

26.(Original) The method according to claim 20, wherein the substrate includes at least two shallow trench electrical isolation regions and further comprising the step of removing selected additional portions of the first film of the electroconductive material covering the shallow trench electrical isolation regions to electrically isolate the cell.

27.(Original) The method according to claim 21, further comprising the step of forming a dielectric Vss spacer along a side wall defined by the floating gate and the protective cap.

28.(Original) The method according to claim 22, further comprising the step of forming a dielectric Vss spacer along a side wall defined by the floating gate and the protective cap.

29.(Original) The method according to claim 23, further comprising the step of forming a dielectric Vss spacer along a side wall defined by the floating gate and the protective cap.

30.(Previously Presented) The method according to claim 18, wherein a dielectric film is disposed between the substrate and the mask film, the trench defining step exposing a portion of the dielectric film at a bottom of the trench.

31.(Previously Presented) The method according to claim 30, further comprising the step of removing the portion of the dielectric film at the bottom of the trench before the trench filling step.

32.(Previously Presented) The method according to claim 31, further comprising the step of forming a coupling film over the exposed portion of the substrate before the trench filling step.

33.(Previously Presented) The method according to claim 18, further comprising the step of removing the mask film.

34.(New) A method of making a flash memory cell comprising a floating gate with corners each having a sharp, upwardly flared shape, the method comprising the steps of:

providing a substrate of semiconductor material;

forming a mask film over the substrate, wherein a dielectric film is disposed between the substrate and the mask film;

defining a trench in the mask film which exposes a portion of the dielectric film at a bottom of the trench, the trench terminating above the substrate;

removing the portion of the dielectric film at the bottom of the trench;

at least partially filling the trench with a first film of electroconductive material; and

etching back a portion of the first film of electroconductive material to form the floating gate with the sharp, upwardly flared corners.